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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/874,032 | 06/06/2001 | Jaroslav Hynecek | ISE107 | 7598 |

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| EXAMINER | |
|---|---|
| TRAN, NHAN T | |
| **ART UNIT** | **PAPER NUMBER** |
| 2615 | |

DATE MAILED: 12/09/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/874,032 | HYNECEK, JAROSLAV | |
| | Examiner | Art Unit | |
| | Nhan T. Tran | 2615 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *27 September 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-3,7-10 and 13-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,7-10 and 13-16* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *27 September 2005* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Specification*

1. A substitute specification filed 9/27/2005 to include priority claim from the provisional application No. 60/245,942 is acknowledged.

### *Drawings*

2. A replacement sheet of drawings was received on 9/27/2005. The drawings are Fig. 2.

### *Response to Arguments*

3. Applicant's arguments filed 9/27/2005 with respect to claims 7-10 & 13-16 have been considered but are moot in view of the new ground of rejection.

4. Applicant's arguments filed 9/27/2005 with respect to claims 1 & 2 have been considered but are not persuasive.

Regarding claim 1, the Applicant asserts, "drawing 400 of the Patent '106 clearly indicates that no MOS gate is present in the region 320 over the punch through transistor region." (remarks, page 8). However, the currently amended claim 1 does not require any MOS gate. *Importantly*, claim 1 recites "the gate" and "the source" which lead to a broad interpretation of any gate and source region of a vertical punch through transistor (VPT) since the claim *does not specifically exclude* any junction gate region that is connected to the source. From this view, the claimed "the gate" is considered as any gate including a junction gate portion of the vertical punch-through transistor as claimed in claim 3 of the Patent '106. For

illustration, the Patent '106 clearly supports the claimed feature in claim 3 in **col. 4, lines 42-45 that the photo-charge sensing VPT transistor 203 (Fig. 2) is formed in the opening 320 (Fig. 4), and the transistor consists of p+ type doped source region 405 that is surrounded and connected to the p+ type doped first junction gate region 404.** It is also seen that the gate (404) being conductively connected to the source (405) since both the gate and source are doped by **the same impurity type (p+)** as claimed in claim 3 of the Patent '106. Thus, the limitation "a vertical punch-through transistor having the gate surrounding the source and being connected to the source." recited in claim 1 is met by claims 1 & 3 of the Patent '106. In addition, claim 7 (a new ground of rejection) is also met by claims 1 & 3 of the Patent '106 for the same reason provided above.

Regarding claim 2, the Applicant states that Kubo Kazuya does not show a vertical punch-through transistor with a gate surrounding its source and being connected to it (remarks, page 9). In response, the Examiner respectfully submits that such feature of the vertical punch-through transistor is taught in the primary reference to the Patent '106. Kubo Kazuya is relied upon for a teaching of a chare present under the gate to modulate the punch through potential barrier of the vertical punch-through transistor (see previous Office Action, pages 6 & 7).

Additionally, the Applicant further states, for claim 10, that Lee does not show any structure similar to present invention of a MOS gate surrounding the source and being connected to it (remarks, page 10). In response, the Examiner respectfully submits the same analysis as in claim 2. Furthermore, claim 10 requires **another gate** (MOS reset gate) coupled to the vertical punch-through transistor to remove charge therefrom, Lee is relied upon for specific teaching of

a MOS reset gate coupled to a transistor to remove charge therefrom in an image sensor (see previous Office Action, pages 8 & 9).

### *Claim Objections*

Claims 1, 7 & 10 are objected to because of the recitation of "..having **the** gate surrounding **the** source and being conductively connected to the source." This limitation should be changed to -- having **a** gate surrounding **a** source and being conductively connected to the source --.

Appropriate correction is required.

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1 & 7 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of **U. S. Patent No. 6,580,106 B2** (hereafter, referred as Patent '106). Although the conflicting claims are not identical, they are not patentably distinct from each other because claims 1 & 7 of the instant application are

encompassed by claims 1 & 3 of the Patent '106. It should be noted that limitation "the gate surrounding the source and being conductively connected to the source" recited in each of claims 1 & 7 of the instant application is met by "the **source** of the vertical punch-through transistor...is **connected** to a first junction **gate** region surrounding the source and doped by the same impurity type as the source and as the substrate." Also, see the Examiner's response to arguments above.

6. Claims 2 & 8 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of the Patent '106 in view of Kubo Kazuya (JP 61-188965).

Regarding claims 2 & 8, the claimed invention of Patent '106 *does not clearly* disclose a charge present under the gate modulates the punch through potential barrier of the vertical punch-through transistor. It is taught by Kubo that a barrier height of a vertical punch through transistor (Fig. 1) is modulated by the charges present under the gate (4, 7) to implant excess charge into substrate 1 for suppressing a blooming, expanding a dynamic range and improving the S/N ratio. See Abstract and Fig. 1.

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to include the feature of modulating the punch through potential barrier of the vertical punch-through transistor by a charge present under the gate for suppressing a blooming, expanding a dynamic range and improving the S/N ratio.

7. Claims 3, 9, 10 & 13-16 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1 and 3 of the Patent '106 and Kubo Kazuya (JP 61-188965) and in further view of Lee et al (US 5,904,493).

Regarding claims 3 & 9, the claimed invention of the Patent '106 and Kubo do not clearly teach a charge reset means adjacent to and coupled to the vertical punch-through transistor to remove charge therefrom. However, as taught by Lee, an image sensor having a charge-sensing transistor (at gate Tx) and a charge reset means (reset gate 24; Fig. 4) adjacent to and coupled to the charge-sensing transistor to remove charge therefrom to avoid anti-blooming (see Lee, col. 3, line 65 – col. 4, line 9).

Therefore, it would have been obvious to one of ordinary skill in the art to provide a charge reset means adjacent to and coupled to the vertical punch-through transistor in the claimed invention of the Patent '106 and Kubo to remove charge therefrom to further improve anti-blooming of charge as taught by Lee.

Regarding claim 10, it is clear that the charge reset means is an MOS reset gate (see Lee, col. 3, line 65 – col. 4, line 9).

Regarding claim 13, see the analyses of claims 1 and 7 for all limitations of claim 13 except for a CCD device. Lee teaches an optimized image sensor that is implemented with best features from both CMOS and CCD technologies. The image sensor improves the blue response

and dark current limitations. The image sensor can be called either as CMOS or CCD device. See Lee, col. 1, lines 45-59.

Therefore, it would have been obvious to one of ordinary skill in the art to construct the image sensor having best features from both CMOS and CCD technologies to improve the blue response and dark current limitations of the image sensor which would be either called as a CMOS or a CCD device.

Regarding claims 14-16, see the analyses of claims 8-10, respectively.

*Conclusion*

8. **Since all currently pending claims 1-3, 7-10 & 13-16 are rejected under obviousness-type double patenting without a separate art rejection under 35 USC 102 or 103, claims 1-3, 7-10 & 13-16 will be allowed if a proper terminal disclaimer is filed.**

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event,

however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nhan T. Tran whose telephone number is (571) 272-7371. The examiner can normally be reached on Monday - Thursday, 7:30am - 5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Ometz can be reached on (571) 272-7593. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

NT.

DAVID OMETZ
SUPERVISORY PATENT EXAMINER